A review of low-noise amplifiers for neural applications

Jesús Ruiz-Amaya, Alberto Rodríguez-Pérez and Manuel Delgado-Restituto
Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC)
Avda. Américo Vespucio S/N, 41092-Sevilla, SPAIN
Email: ruiz|alberto|mandel@imse-cnm.csic.es

Abstract **– This paper presents a comparative study of three low-noise amplifiers for neural recording applications. The topologies are thoroughly analysed in terms of area, power consumption and noise performance. Further, the theoretical results are confirmed by simulations of transistor-level implementations in a 0.13μm CMOS technology at 1.2V supply voltage.**

Index Terms **– Amplifier, low power, low noise, neural recording, biomedical applications.**

I. Introduction.

During the last years, there has been a growing interest on the design of neural recording interfaces with wireless transmission capabilities for the untethered measurement of brain activity [1-3]. These interfaces are expected to play a significant role both in clinical (as part of therapeutic procedures in patients with neurological diseases) and neuroscience applications. These systems are essentially composed by a set of microelectrodes to capture the neural activity, followed by a bank of low-noise amplifiers (LNAs) for signal conditioning and a mixed-signal circuitry to digitize and process the acquired data prior to wireless transmission. A key element in this architecture is the LNA which must be able to boost the weak signals detected by the microelectrodes and filter out the undesired frequency components, under severe area and power consumption constraints.

Different proposals can be found in the literature to efficiently solve the challenging noise-power-area trade-off demanded by neural LNAs [4-7]. In this paper, three of these approaches are reviewed and evaluated, paying special attention to their noise performances. Focus will be made in those realizations targeting the detection of action potential-generated spikes [8]. The frequency content of the spike generation activity ranges from about 200Hz to 7kHz and the peak amplitude of the waveforms are typically of the order of about 1mV (it depends on a number of factors, including electrode geometry and proximity to a cell body). LNAs for this application often require mid-band gains of 40dB or higher, an input-referred noise level in the order of $3\mu V_{rms}$ and an effective resolution above 7 bits.

After presenting the three approaches in Section II, Section III shows the performance of corresponding transistor-level realizations in a 0.13μm CMOS technology for a 1.2V supply voltage. At the light of the theoretical treatment and the electrical simulations presented in the previous sections, Section IV summarizes the results of the comparative study.

II. Low Noise Amplifier Topologies

Table I shows the three topologies for neural spike recording considered for analysis. They are referred to as Capacitive Feedback Network (CFN) [1],[2],[5],[7], Miller Integrator Feedback Network (MIFN) [4] and Capacitive Amplifier Feedback Network (CAFN) [6] amplifiers. Assuming that all the Operational Transconductance Amplifiers (OTAs) are described by single-pole networks†, the transfer functions of the three topologies are given by:

$$H_{CFN}(s) \approx \frac{G(1+s/z_H)s}{(1+s/p_L)(1+s/p_H)}$$
$$H_{MIFN}(s) \approx \frac{G(1+s/z_L)}{(1+s/p_L)(1+s/p_H)} \qquad (1)$$
$$H_{CAFN}(s) \approx \frac{Gs}{(1+s/p_L)(1+s/p_H)}$$

where the poles (p_L, p_H), zeros (z_L, z_H) and DC gains (G) are defined in the second column of Table I under the usual assumptions expressed in the third column. The transfer functions in (1) have bandpass characteristics with a passband midgain, A_m, also defined in the second column of Table I. The fourth column gives expressions for the input-referred thermal noise††, V_{rms}, of the three structures, taking into account the contributions from the OTAs and the feedback resistors, R_f. Parameter n stands for the transistor slope factor [9] and γ amounts 1 for single-ended and 2 for fully-differential amplifiers.The fourth column of Table I also includes expressions for the theoretical limit of the LNA noise efficiency factor defined as [10]:

$$NEF = V_{rms}\sqrt{\frac{2I_{tot}}{\pi \cdot U_t \cdot 4kT \cdot BW}} \qquad (2)$$

†. OTAs are characterized by their transconductances, g_{mx}; output resistances, g_{ox}; capacitances C_{pix}, C_{pox} at the input and output terminals, respectively; and noise excess factors η_x [11]. Sub-index $x = 1, 2$ points out to amplifiers A_1 or A_2.

††. This paper focuses exclusively on thermal noise contributions. Flicker noise may also impact in the noise characteristics of the LNAs, but it can be substantially reduced by using chopper or auto-zero techniques.

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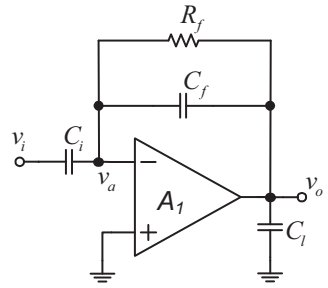
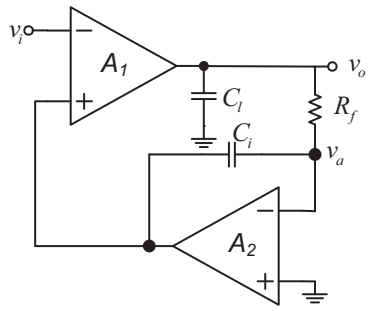
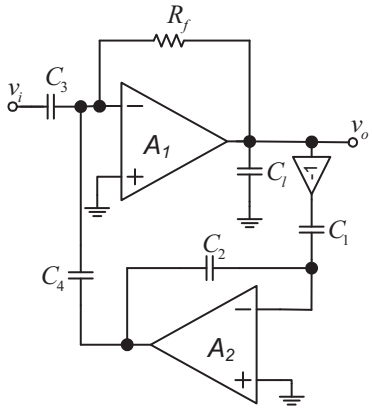
TABLE I. NEURAL AMPLIFIERS PERFORMANCE SUMMARY.

Topology	Poles & Zeros Midband gain	Assumptions & Parameter Definitions	Noise performance
 **Fig. 1.** CFN topology.	$G = -C_i R_f$ $z_L = 0$ $z_H = -g_{m1}/C_f$ $p_L \approx \frac{-1}{R_f C_f}$ $p_H \approx \frac{-g_{m1}}{A_m C_{t1}}$ $A_m = -C_i/C_f$	$A_o\beta \gg 1$ $A_m \gg 1$ $C_{t1} = C_l + C_{po1}$ $\beta = C_f/(C_{pi1} + C_i + C_f)$	**Input-referred noise** V_{rms} $\sqrt{\gamma\frac{KT}{A_m}\left(\frac{1}{C_i}+\frac{n}{2C_{t1}}(1+\eta_1)\right)}$ **Minimum theoritical NEF** $n\sqrt{\gamma k_1(1+\eta_1)}$
 **Fig. 2.** MIFN topology.	$G = -1/A_{o2}$ $z_L \approx \frac{-1}{A_{o2}C_i R_f}$ $p_L \approx -\frac{A_m}{R_f C_i}$ $p_H \approx -\frac{g_{m1}}{A_m C_{t1}}$ $A_m = -A_{o1}$	$g_{m1}R_f \gg 1 \quad g_{m2}R_f \gg 1$ $A_{o1} \gg 1 \quad A_{o2} \gg 1$ $g_{m2}/C_{eq2} \gg p_H$ $C_{t1} = C_l + C_{po1}$ $C_{t2} = C_{po2} + C_{pi1}$ $C_{eq2} = C_{pi2} + C_i + C_{t2}/\beta$ $\beta = C_i/(C_{pi2} + C_i)$	**Input-referred noise** V_{rms} $\sqrt{\gamma\frac{KT}{A_m}\left(\frac{1}{C_i}+\frac{n}{2C_{t1}}(1+\eta_1+\psi_2)\right)}$ $\psi_2 = \frac{g_{m1}(1+\eta_2)}{\beta^2 g_{m2}}$ **Minimum theoritical NEF** $NEF_{CFN}\left(1+\frac{1}{\beta}\sqrt{\frac{k_2}{k_1}\frac{1+\eta_2}{1+\eta_1}}\right)$
 **Fig. 3.** CAFN topology.	$G = -R_f C_3$ $z_L = 0$ $p_L \approx \frac{-C_2}{C_1 C_4 R_f}$ $p_H \approx -\frac{g_{m1}}{A_m C_{t1}}$ $A_m \approx -\frac{C_3 C_2}{C_1 C_4}$	$g_{m1}R_f \gg 1 \quad g_{m2}R_f \gg 1$ $A_{o1} \gg (C_2 C_{n1})/(C_1 C_4)$ $A_{o2} \gg 1$ $g_{m2} \gg \frac{g_{m1} C_1 C_4}{C_{t1} C_{n1}}$ $C_{n1} = C_3 + C_4 + C_{p1}$ $C_{eq2} = C_{pi2} + C_1 + (C_4 + C_{t2})/\beta_2$ $C_{t1} = C_l + C_{po1}$ $C_{t2} = C_{po2}$ $\beta_2 = C_2/(C_{pi2} + C_1 + C_2)$	**Input-referred noise** V_{rms} $\sqrt{\gamma\frac{KT}{A_m}\left(\frac{1}{C_3}+\frac{n}{2C_{t1}}(1+\eta_1+\psi_2)\right)}$ $\psi_2 = \frac{g_{m1}(1+\eta_2)}{\beta_2^2 g_{m2}}\left(\frac{C_4}{C_3}\right)^2$ **Minimum theoritical NEF** $NEF_{CFN}\sqrt{1+\frac{k_2}{k_1}\frac{g_{m2}}{g_{m1}}}$

where I_{tot} is the total supply current of the LNA, $U_t = KT/q$ is the thermal voltage, and BW stands for the LNA bandwidth which is essentially determined by the high-frequency pole, p_H, as

$$BW = g_{m1}/(2\pi A_m C_{t1}) \tag{3}$$

In the following, such NEF theoretical limits are explicitly derived for each LNA topology.

A. NEF for the CFN LNA

Assuming that the input differential pair of the OTA is biased in weak inversion with a tail current, I_{ota1}, the total supply current of the CFN LNA can be approximated by the expression

$$I_{tot} = I_{ota1} = k_1 n g_{m1} U_t(\sqrt{1+IC_1}+1) \tag{4}$$

where k_1 is an OTA-topology factor, and IC_1 is the inversion coefficient [12]. Replacing (3) and (4) into (2), taking also into account the expression for the input referred noise, V_{rms}, in Table I, it can be found that

$$NEF_{CFN} \approx \sqrt{n\gamma k_1\left(2\frac{C_{t1}}{C_i} + n(1+\eta_1)\right)} \tag{5}$$

where it has been assumed that $IC_1 \ll 1$. Given that typically $C_i \gg C_{t1}$, the above expression can be further approximated as,

$$NEF_{CFN} \approx n\sqrt{\gamma k_1(1+\eta_1)} \tag{6}$$

B. NEF for the MIFN LNA

In this topology, the total supply current is determined by the sum of the current consumptions of the

two OTAs. Assuming weak inversion operation,

$$I_{tot} = I_{ota1} + I_{ota2} \approx 2(k_1 + \alpha k_2) n g_{m1} U_t \qquad (7)$$

where $\alpha = g_{m2}/g_{m1}$ and the last approximation assumes low inversion coefficients, $IC_1, IC_2 \ll 1$. Replacing (3) and (7) into (2), and taking into account the input referred noise, V_{rms}, in Table I, it can be found that

$$NEF_{MIFN} \approx n\sqrt{\gamma(k_1+\alpha k_2)(1+\eta_1+\psi_2)} \qquad (8)$$

where it has been assumed that $C_i \gg C_{t1}$. This expression is minimized if the transconductance ratio satisfies the condition:

$$\alpha = \frac{1}{\beta}\sqrt{\frac{k_1}{k_2}\frac{(1+\eta_2)}{(1+\eta_1)}} \qquad (9)$$

Replacing (9) into (8), the minimum noise efficiency is thus given by:

$$NEF_{MIFN} \approx NEF_{CFN}\chi_{MIFN} \qquad (10)$$

where χ_{MIFN} is a exceeding factor respect the CFN topology given by

$$\chi_{MIFN} = 1 + \frac{1}{\beta}\sqrt{\frac{k_2}{k_1}\frac{(1+\eta_2)}{(1+\eta_1)}} \qquad (11)$$

C. NEF for the CAFN LNA

As can be observed in Table I, in this topology the noise contribution of amplifier A_2 is divided by a factor $(C_3/C_4)^2$. Therefore, a large C_3 value must be chosen for decreasing noise. Under this condition, CAFN exhibits a performance similar to the CFN architecture with a NEF given by,

$$NEF_{CAFN} \approx NEF_{CFN}\chi_{CAFN} \qquad (12)$$

where χ_{CAFN} is again a exceeding factor respect the CFN topology given by

$$\chi_{CAFN} = \sqrt{1 + \frac{k_2}{k_1}\frac{g_{m2}}{g_{m1}}} \qquad (13)$$

III. Transistor-Level Exploration

In order to quantify the pros and cons of the previous LNA topologies, we have realized a transistor-level exploration of the architectures in a 0.13µm CMOS technology. Common design objectives for the three topologies, assumed single-ended, are a midband gain of 47dB and an operation bandwidth from 250Hz to 7kHz. In all cases, high DC-gain OTAs must be used to satisfy the assumptions in Table I. A cascode current mirror amplifier [see Fig. 4(a)] has been used to implement A_1 OTAs, given its simplicity and relatively high DC gain and output swing; whereas a less noisy telescopic amplifier [see Fig. 4(b)] has been considered to implement A_2 OTAs. This also allows for a fair comparison of the LNAs topologies in terms of thermal noise behavior. Note that OTA-related parameters are $\eta_1 \approx 1.5$ and $k_1 = 2$ for the current mirror amplifier, and $\eta_2 \approx 0.5$ and $k_2 = 1$ for the telescopic OTA.

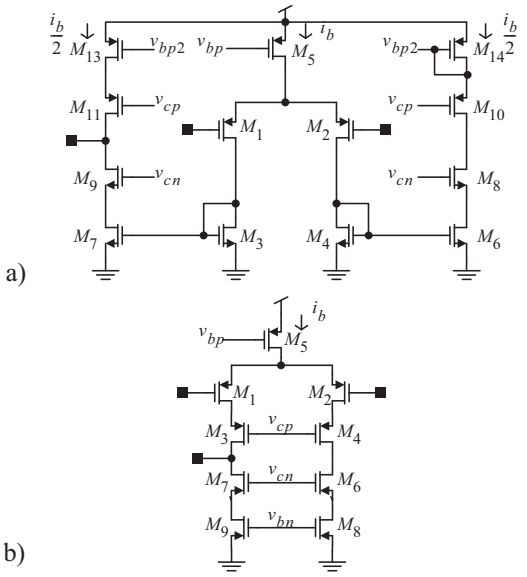


Fig. 4. OTAs considered for the transistor-level implementation of the LNAs: (a) current mirror OTAand (b) telescopic OTA.

Given these target specifications, the transistor-level exploration (applied to each LNA topology) has consisted on identifying that configuration which obtains the minimum area occupation for a given input-referred noise value. Additionally, the NEF is constrained to be no higher than 8% the minimum theoretical NEF derived in Section II. It is worth noting that, for a fixed bandwidth and noise level, a low NEF value also implies a reduced power consumption according to (2).

As an illustration, Fig. 5 depicts the transistor-level synthesis routine used for the CFN LNA (similar algorithms have been also developed for the other LNAs). The procedure uses as design variables the feedback, C_f, and load, C_l, capacitances, and the inversion coefficient of the amplifier IC_1. These variables also act as running parameters in a optimization loop which evaluates at every iteration the accomplishment of the target specifications and select that valid configuration with the minimum power consumption. The sizing procedure starts by guessing initial values for the OTA parasitic capacitances, C_{pi1}, C_{po1}, and DC-gain, A_{o1}. Using these values, the feedback factor, β, and equivalent closed-loop capacitance, C_{eq1}, are computed and, thereafter, the transcondutance, g_{m1}, and feedback resistor, R_f, based on bandwidth specifications†. A transistor-level sizing routine, similar to that reported in [13], is then run to accurately estimate transistor sizes, bias currents and other electrical-level parameters of the LNA. This routine uses look-up tables of technology parameters, obtained from batches of electrical-level simulations, to complete the sizing task. At this point, the overall power consump-

†. In the MIFN and CAFN topologies, g_{m2} must be also computed. For the MIFN architecture, g_{m2} can be obtained according to (9), whereas for the CAFN topology, g_{m2} must satisfy the assumption in Table I, i.e., $g_{m2} \approx n g_{m1} C_1 C_4/(C_{t1} C_{n1})$ with n a scaling factor much higher than unity (values around 10 are enough for most practical purposes).

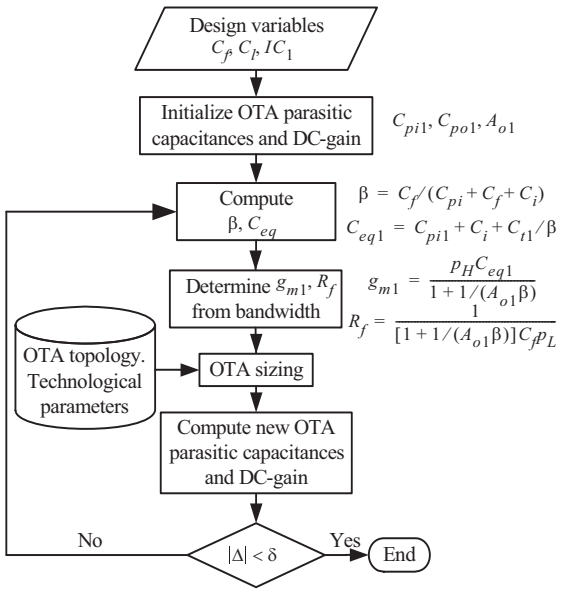


Fig. 5. Synthesis procedure for the CFN LNA.

tion of the OTA, area, parasitics and DC-gain can be calculated. These values for the parasitics and DC-gain are compared to those originally estimated at the beginning of the procedure. If discrepancies (Δ) are higher than a user-defined tolerance value, (δ), the procedure is repeated again until convergence is reached.

The results of the exploration are shown in Fig. 6, in which the power and area consumptions of the optimum solutions, as well as their *NEFs*, are represented against the input-referred noise. Plots are obtained from electrical simulations of the final configurations derived with the aforementioned synthesis routines. It is worth mentioning that according to our synthesis procedures and the calculated OTA-related parameters (k_1, k_2, η_1, η_2), the exceeding NEF factors for the MIFN, χ_{MIFN}, and CAFN, χ_{CAFN}, topologies are respectively, around 1.5 and 1. Hence the fact that *NEFs* remain close for the CFN and CAFN LNAs whereas the MIFN LNA presents a higher value. Also observe that, for a given input-referred noise, the CFN topology performs better in terms of area and power consumptions, contrary to what is claimed elsewhere [4], [6].

Although the exploration has been realized for single-ended LNA topologies, similar conclusions can be drawn in the case of fully-differential structures, more suitable for low-voltage environments.

IV. Conclusions.

This paper compares the performance of three LNA topologies for neural spike recording applications. The study, based upon theoretical developments and transistor-level explorations, reveals that the CFN approach [1],[2],[5],[7] achieves the best performance in terms of area and power consumptions for a given input-referred noise specification.

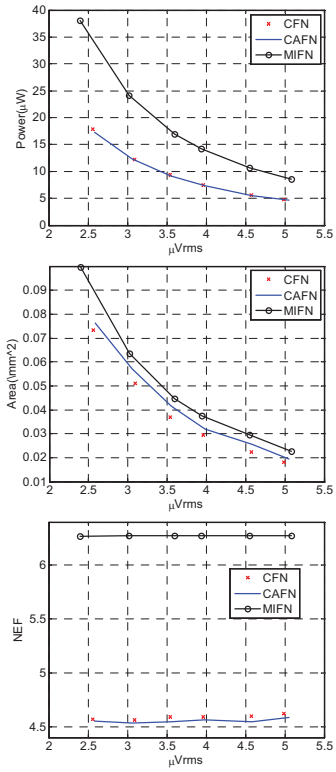


Fig. 6. Results from the transistor-level exploration.

Acknowledgments

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